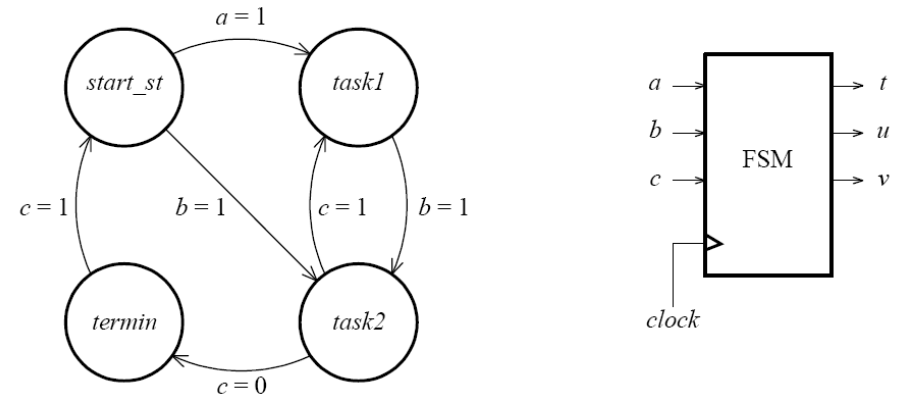
**Assignment 2 Coursework Specification**

|  |  |  |
| --- | --- | --- |
| Module Name: | Advanced Digital Design | |
| Module Code: | ENGD3001 | |
| Title of the Assignment: | Assignment 2 | |
| This coursework item is: | | Formative |
| This coursework will be marked anonymously: | | Yes |
| The module learning outcomes that are assessed by this coursework are:   1. “Knowledge and specialist analytic development techniques in the areas of VLSI design, ASM design and implementation, and VHDL design.” 2. “Development of generic and transferable skills in advanced digital system design methodologies using industry standard design tools.” | | |
| This coursework is: | | Individual |
| This coursework constitutes 24% to the overall module mark. | | |
| Date Set: | by DMU | |
| Date & Time Due: | by 4:00 PM on Friday, 15 Jan 2021 | |
| **When completed you are required to submit the following:**   1. **Submit an electronic copy of your assignment to TURNITIN via Blackboard by the advertised deadline.**   **IMPORTANT: Partial submissions are not acceptable. Failure to submit the electronic copy to Turnitin amounts to a non-submission.** | | |
| **Your marked coursework and feedback will be available to you on:**  If for any reason this is not forthcoming by the due date your module leader will let you know why and when it can be expected | | 15 Feb 2021 |
| **Late submission of coursework policy:**  Late submissions will be processed in accordance with current University regulations which state:  *“The time period during which a student may submit a piece of work late without authorisation and have the work capped at 40% [50% at PG level] if passed is* ***14 calendar days****. Work submitted unauthorised more than 14 calendar days after the original submission date will receive a mark of 0%. These regulations apply to a student’s first attempt at coursework. Work submitted late without authorisation which constitutes reassessment of a previously failed piece of coursework will always receive a mark of 0%.”* | | |
| **Academic Offences and Bad Academic Practices:**  These include plagiarism, cheating, collusion, copying work and reuse of your own work, poor referencing or the passing off of somebody else's ideas as your own. If you are in any doubt about what constitutes an academic offence or bad academic practice you must check with your tutor. Further information and details of how DSU can support you, if needed, is available at:  <https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/academic-offences.aspx>  and  <https://www.dmu.ac.uk/current-students/student-support/exams-deferrals-regulations-policies/student-regulations-and-policies/bad-academic-practice.aspx> | | |
| Module leader/ tutor name: | Mr. G.H. Rohan O. Dharmarathna | |
| Contact details: | [rohan.dharmarathna@dmu.ac.uk](mailto:rohan.dharmarathna@dmu.ac.uk) | |

**Assignment 2**

The figure below shows the state transition diagram of a finite state machine (FSM). This diagram shows the input conditions which initiate the necessary transitions. If no input condition is satisfied, then the FSM remains in the same state.



The outputs of the FSM are defined in the following table:

|  |  |  |  |
| --- | --- | --- | --- |
| **State** | **t** | **u** | **v** |
| *start\_st* | 0 | 0 | 0 |
| *task1* | 0 | 1 | 0 |
| *task2* | 1 | 1 | 0 |
| *termin* | 1 | 1 | 1 |

Implement this FSM in VHDL and simulate its behaviour **with the aid of a text-based testbench (a testbench written in VHDL)**. Please ensure that you design your testbench in such a way that it verifies all possible states/transitions from the above diagram.

**What you should submit**

You should submit a formal report explaining your design and your results. For general guidance on writing (technical) reports please refer to the following link:

[*https://www.theiet.org/media/5182/technical-report-writing.pdf*](https://www.theiet.org/media/5182/technical-report-writing.pdf)

Specifically, your report should contain at least:

1. an introduction including the design brief,
2. a background section,
3. a section explaining how you’ve solved the design task given to you and if applicable why you’ve selected a particular solution out of several possible,
4. the complete listing of the code you’ve written, **bearing in mind good programming and design practice**,
5. the results of the simulations carried out (i.e. suitable, legible, and detailed simulation waveforms)
6. accompanied by detailed comments and explanations, and
7. conclusions (and possible further improvements if applicable). Avoid including simulation waveforms with a black background.

***For full marking details please consult the associated marking scheme on Blackboard****.*